We claim:

SUB Q4 1. A method for making a programmable resistance memory element, comprising:

providing a conductive material;

forming a sidewall spacer over a portion of said conductive material;

removing a portion of said conductive material to form a raised portion extending from said conductive material under said spacer; and

forming a programmable resistance material adjacent to at least a portion of said raised portion.

2. The method of claim 1, wherein said removing step comprises etching said conductive material.

3. The method of claim 2, wherein said etching step comprises anisotropically etching said conductive material.

4. The method of claim 2, wherein said etching step comprises isotropically etching said conductive material.

5. The method of claim 1, wherein said forming said sidewall spacer step comprises:

forming a first layer over said conductive material;

forming a second layer over said first layer;

forming a sidewall surface in said second layer;

forming a third layer over said sidewall surface;

removing a portion of said third layer;

removing said second layer; and

removing a portion of said first layer.

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6. The method of claim 5, wherein said forming said sidewall surface step, comprises:

forming a forth layer over said second layer;

removing a portion of said forth layer; and

removing a portion of said second layer to form said sidewall surface in said second layer.

7. The method of claim 5, wherein said removing said portion of said third layer step comprises anisotropically etching said third layer.

8. The method of claim 5, wherein said removing said portion of said first layer comprises anisotropically etching said first layer.

9. The method of claim 5, wherein said first and third layers are oxides.

10. The method of claim 5, wherein said second layer is polysilicon.

11. The method of claim 5, wherein said first and third layers are nitrides.

12. The method of claim 5, wherein said second layer is an oxide.

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13. The method of claim 6, wherein said forth layer is a photoresist.

14. The method of claim 1, wherein said sidewall spacer comprises a material selected from the group consisting of dielectric, semiconductor, and conductor.

15. The method of claim 1, wherein said sidewall spacer comprises a material selected from the group consisting of oxide and nitride.

16. The method of claim 1, wherein said sidewall spacer comprises polysilicon.

17. The method of claim 1, wherein said programmable resistance material comprises a phase change material.

18. The method of claim 1, wherein said programmable resistance material comprises a chalcogen element.

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19. A method for making a programmable resistance memory element, comprising:

providing a conductive layer;

forming a raised portion extending from an edge of said conductive layer; and

forming a programmable resistance material adjacent to at a least a portion of said raised portion.

20. The method of claim 19, wherein said forming said raised portion step comprises:

forming a mask over a portion of said edge; and

removing a portion of said conductive layer to form said raised portion under said mask.

21. The method of claim 20, wherein said removing step comprises etching said conductive layer.

22. The method of claim 21, wherein said etching step comprises anisotropically etching said conductive layer.

23. The method of claim 21, wherein said etching step comprises isotropically etching said conductive layer.

24. The method of claim 20, wherein said mask has a lateral dimension less than 1000 Angstoms.

25. The method of claim 20, wherein said mask is a sidewall spacer and forming said mask step comprises forming said sidewall spacer.

26. The method of claim 25, wherein said forming said sidewall spacer step comprises:

forming a first layer over said edge;

forming a second layer over said first layer;

forming a sidewall surface in said second layer;

forming a third layer over said sidewall surface;

removing a portion of said third layer;

removing said second layer; and

removing a portion of said first layer.

27. The method of claim 26, wherein said forming said sidewall surface step, comprises:

forming a forth layer over said second layer;

removing a portion of said forth layer; and

removing a portion of said second layer to form said sidewall surface in said second layer.

28. The method of claim 26, wherein said removing said portion of said third layer step comprises anisotropically etching said third layer.

29. The method of claim 26, wherein said removing said portion of said first layer comprises anisotropically etching said first layer.

30. The method of claim 26, wherein said first and third layers are oxides.

31. The method of claim 26, wherein said second layer is polysilicon.

32. The method of claim 26, wherein said first and third layers are nitrides.

33. The method of claim 26, wherein said second layer is an oxide.

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34. The method of claim 27, wherein said forth layer is a photoresist.

35. The method of claim 19, wherein said forming said memory material step comprises forming said memory material adjacent to a

top surface of said raised portion.

36. The method of claim 19, wherein the step of providing said conductive layer comprises:

providing a dielectric layer;

forming a sidewall surface in said dielectric layer; and

forming said conductive layer on said sidewall surface.

SUB Q39

37. The method of claim 19, wherein conductive layer is a conductive sidewall layer or a conductive sidewall liner.

38. The method of claim 19, wherein said programmable resistance material comprises a phase change material.

39. The method of claim 19, wherein said programmable resistance material comprises a chalcogen element.

SUB Q40

40. A method of forming a programmable resistance memory element, comprising:

providing a first dielectric layer;

forming a sidewall surface in said dielectric layer;

forming a conductive layer on said sidewall surface;

forming a second dielectric layer over said conductive layer;

forming or exposing an edge of said conductive layer;

forming a raised portion extending from said edge of said

conductive layer; and

forming a programmable resistance material adjacent to at least a portion of said raised portion.

41. The method of claim 40, wherein said forming said raised portion step comprises:

forming a mask over a portion of said edge; and

removing a portion of said conductive layer to form said raised portion under said mask.

42. The method of claim 41, wherein said removing step comprises etching said conductive layer.

43. The method of claim 42, wherein said etching step comprises anisotropically etching said conductive layer.

44. The method of claim 42, wherein said etching step comprises isotropically etching said conductive layer.

45. The method of claim 41, wherein said mask has a lateral dimension less than 1000 Angstroms.

46. The method of claim 41, wherein said mask is a sidewall spacer and forming said mask step comprises forming said sidewall spacer.

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47. The method of claim 46, wherein said forming said sidewall spacer step comprises:

forming a first layer over said edge;

forming a second layer over said first layer;

forming a sidewall surface in said second layer;

forming a third layer over said sidewall surface;

removing a portion of said third layer;

removing said second layer; and

removing a portion of said first layer.

48. The method of claim 47, wherein said forming said sidewall surface step, comprises:

forming a forth layer over said second layer;

removing a portion of said forth layer; and

removing a portion of said second layer to form said sidewall surface in said second layer.

49. The method of claim 47, wherein said removing said portion of said third layer step comprises anisotropically etching said third layer.

50. The method of claim 47, wherein said removing said portion of said first layer comprises anisotropically etching said first layer.

51. The method of claim 47, wherein said first and third layers are oxides.

52. The method of claim 47, wherein said second layer is polysilicon.

53. The method of claim 47, wherein said first and third layers are nitrides.

54. The method of claim 47, wherein said second layer is an oxide.

55. The method of claim 48, wherein said forth layer is a photoresist.

56. The method of claim 40, wherein said forming said programmable resistance material step comprises the steps of:

forming a third dielectric layer on said edge and over said raised portion;

removing a portion of said third dielectric layer to expose a top surface of said raised portion; and

forming said programmable resistance material over at least a portion of said top surface.

57. The method of claim 40, wherein said forming said sidewall surface step comprises forming an opening in said first dielectric layer, said opening having said sidewall surface.

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58. The method of claim 57, wherein forming said conductive layer on said sidewall surface step comprises forming said conductive layer on said sidewall surface and said bottom surface of said opening.

59. The method of claim 40, further comprising:

after said forming said conductive layer step and before said forming said second dielectric layer step, removing a portion of said conductive layer.

60. The method of claim 59, wherein said removing said conductive layer step comprises anisotropically etching said conductive layer.

61. The method of claim 40, wherein said programmable resistance material comprises a phase change material.

62. The method of claim 40, wherein said programmable resistance material comprises a chalcogen element.

SUB A15

63. A method for making an electrode for a semiconductor device,

comprising:

providing a conductive layer; and

forming a raised portion extending from an edge of said conductive layer.

64. The method of claim 63, wherein said forming said raised portion step comprises:

forming a mask over a portion of said edge; and

removing a portion of said conductive layer to form said raised portion under said mask.

65. The method of claim 64, wherein said removing step comprises etching said conductive layer.

66. The method of claim 65, wherein said etching step comprises anisotropically etching said conductive layer.

67. The method of claim 65, wherein said etching step comprises isotropically etching said conductive layer.

68. The method of claim 64, wherein said mask has a lateral dimension less than 1000 Angstoms.

69. The method of claim 64, wherein said mask is a sidewall spacer and forming said mask step comprises forming said sidewall

spacer.

70. The method of claim 69, wherein said forming said sidewall spacer step comprises:

forming a first layer over said edge;

forming a second layer over said first layer;

forming a sidewall surface in said second layer;

forming a third layer over said sidewall surface;

removing a portion of said third layer;

removing said second layer; and

removing a portion of said first layer.

71. The method of claim 70, wherein said forming said sidewall surface step, comprises:

forming a forth layer over said second layer;

removing a portion of said forth layer; and

removing a portion of said second layer to form said sidewall surface in said second layer.

72. The method of claim 70, wherein said removing said portion of said third layer step comprises anisotropically etching said third layer.

73. The method of claim 70, wherein said removing said portion of said first layer comprises anisotropically etching said first

layer.

74. The method of claim 70, wherein said first and third layers are oxides.

75. The method of claim 70, wherein said second layer is polysilicon.

76. The method of claim 70, wherein said first and third layers are nitrides.

77. The method of claim 70, wherein said second layer is an oxide.

78. The method of claim 71, wherein said forth layer is a photoresist.

79. The method of claim 63, wherein said forming said memory material step comprises forming said programmable resistance material adjacent to a top surface of said raised portion.

80. The method of claim 63, wherein the step of providing said conductive layer comprises:

providing a dielectric layer;

forming a sidewall surface in said dielectric layer; and

forming said conductive layer on said sidewall surface.

81. The method of claim 63, wherein conductive layer is a conductive sidewall layer or a conductive sidewall liner.

82. A method of making an electrode for a semiconductor device, comprising:

providing a first dielectric layer;

forming a sidewall surface in said dielectric layer;

forming a conductive layer on said sidewall surface;

forming a second dielectric layer over said conductive layer;

forming or exposing an edge of said conductive layer; and

forming a raised portion extending from said edge of said conductive layer.

83. The method of claim 82, wherein said forming said raised portion step comprises:

forming a mask over a portion of said edge; and

removing a portion of said conductive layer to form said raised portion under said mask.

84. The method of claim 84, wherein said removing step comprises etching said conductive layer.

85. The method of claim 84, wherein said etching step comprises anisotropically etching said conductive layer.

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86. The method of claim 84, wherein said etching step comprises isotropically etching said conductive layer.

87. The method of claim 83, wherein said mask has a lateral dimension less than 1000 Angstoms.

88. The method of claim 83, wherein said mask is a sidewall spacer and forming said mask step comprises forming said sidewall spacer.

89. The method of claim 88, wherein said forming said sidewall spacer step comprises:

forming a first layer over said edge;

forming a second layer over said first layer;

forming a sidewall surface in said second layer;

forming a third layer over said sidewall surface;

removing a portion of said third layer;

removing said second layer; and

removing a portion of said first layer.

90. The method of claim 89, wherein said forming said sidewall surface step, comprises:

forming a forth layer over said second layer;

removing a portion of said forth layer; and

removing a portion of said second layer to form said sidewall surface in said second layer.

91. The method of claim 89, wherein said removing said portion of said third layer step comprises anisotropically etching said third layer.

92. The method of claim 89, wherein said removing said portion of said first layer comprises anisotropically etching said first layer.

92. The method of claim 89, wherein said first and third layers are oxides.

94. The method of claim 89, wherein said second layer is polysilicon.

95. The method of claim 89, wherein said first and third layers are nitrides.

96. The method of claim 89, wherein said second layer is an oxide.

97. The method of claim 90, wherein said forth layer is a photoresist.

98. The method of claim 82, wherein said forming said programmable resistance material step comprises the steps of:

forming a third dielectric layer on said edge and over said raised portion; and

removing a portion of said third dielectric layer to expose a top surface of said raised portion.

99. The method of claim 82, wherein said forming said sidewall surface step comprises forming an opening in said first dielectric layer, said opening having said sidewall surface.

100. The method of claim 99, wherein forming said conductive layer on said sidewall surface step comprises forming said conductive layer on said sidewall surface and said bottom surface of said opening.

101. The method of claim 82, further comprising:

after said forming said conductive layer step and before said forming said second dielectric layer step, removing a portion of said conductive layer.

102. The method of claim 101, wherein said removing said conductive layer step comprises anisotropically etching said conductive layer.